

**ABSTRACT:****REDUCED POWER CONSUMPTION SIGNAL PROCESSING  
METHODS AND APPARATUS**

This invention is generally concerned with reduced power consumption signal processing methods and apparatus, and in particular with techniques for jointly controlling power supply voltage and clock frequency in a receiver to reduce power consumption.

A method of reducing the power consumption of a data receiver is described. The receiver is configured to process a received signal using repeated implementations of substantially the same first data processing element, a rate of said repetitions being determined by a clock frequency of said first data processing element. The method comprises determining a number of repetitions of said repeated implementations of said first data processing element; processing said receiving signal according to said determined number of repetitions; adjusting said number of repetitions in response to a power saving control signal; and jointly reducing said clock frequency and a power supply voltage to said first data processing element in response to said control signal to reduce said receiver power consumption.

Figure 5.